IMPEDANCE MATCHING TECHNIQUES FOR RF & MICROWAVE CIRCUIT DESIGN

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OVERVIEW

The need to match impedance is unavoidable by anyone working in RF. Power transistors are not 50 Ω input and optimum loads at the transistor output are not 50 Ω. Optimum noise match impedance at a LNA FET input is not 50 Ω. This paper presents techniques to first, design lumped LC circuits for impedance matching. Next, a straightforward technique to convert a lumped design into a printed circuit realizable form is presented.

Bandwidth needs for amateur radio are relatively low; perhaps 10% or less. Techniques to broadband match over an octave (or more) use synthesis techniques. For those readers interested in broadband synthesis, please read my paper on that subject: http://k5tra.net/TechFiles/Broadband.pdf .

Q·BW LIMITS TO MATCH PERFORMANCE

The Q of the load sets natural limits to the achievable impedance match. The best possible match reflection coefficient is limited by the product of load Q and BW, the % bandwidth. This is expressed mathematically as: $\rho \geq e^{\left(\frac{-\pi}{Q*BW}\right)}$.

In terms of this reflection coefficient, SWR is expressed as: $SWR = (1+\rho)/(1-\rho)$.

This best case match performance is represented graphically in Fig.1. The curves indicate ideal performance limits not practically achievable; but serve as a useful bound for expectations. That said, a 1.05:1 SWR ideal limiting case could easily correspond to an SWR of 1.1:1 or more in a practical finite order circuit. So, for a 10% BW match, the load Q shouldn't be greater than 8. A load Q greater than 8 will require a match bandwidth less than 10% for the same match performance.

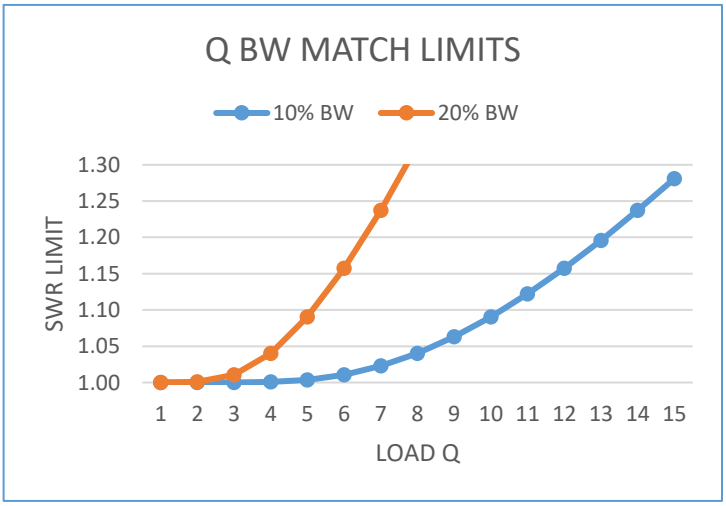


Figure 1 Ideal limit to match

TWO ASPECTS OF IMPEDANCE MATCHING

Transformers and impedance transforming networks are an important part of impedance matching. It would be unusually fortunate to need a match to a purely resistive load. Usually, the load impedance is complex; so, transformer action and reactance (or susceptance) absorption is required from the circuit. In most narrow band cases, impedance matching can

be thought of as resonating the reactance (or susceptance) followed by the necessary transformer action to match the source resistance (often 50Ω).

The primary approach to the design of lumped element matching circuits will be based on the Smith Chart. For completeness, I would like to first like to briefly discuss use of several non-LC impedance transformers in matching networks. If the reactive part of the load impedance is resonated with an opposite series reactance, then the remaining task is to simply cascade an appropriate transformer. The same is true if the load is viewed as a parallel RC or RL, where an opposite susceptance is added to resonate the load and an appropriate transformer is cascaded. Several obvious transformers are quarter-wave transmission lines or short coupled-line transmission line structures such as Ruthroff or Guanella transformers. For a thorough presentation of these topics, please read my paper on that subject: http://k5tra.net/TechFiles/Transformers.pdf .

THE SMITH CHART

The easiest way to design narrow band impedance matching circuits is with the Smith Chart. It is an extremely useful graphical tool that unfortunately is viewed as “mysterious” to the uninitiated. A bit of explanation will hopefully remove the mystery. First, consider Fig. 2. The reflection coefficient, ρ, is the ratio of reflected to forward voltage at the load. It is a complex number representable as either (real, imaginary) or (magnitude, angle). The maximum magnitude of reflection with passive loads is 1.0 (total reflection). This is plotted as the unit circle in Fig. 2 and represents the outer boundary of the standard smith chart.

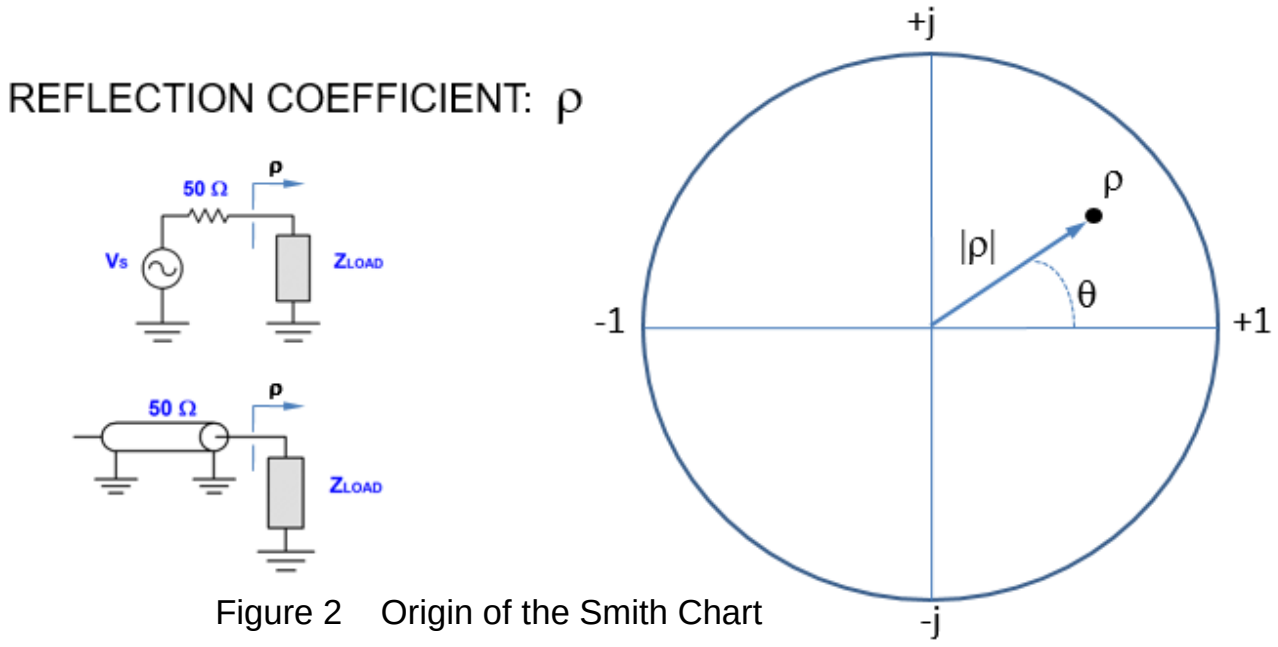


Figure 2 Origin of the Smith Chart

In other words, ALL possible passive reflection coefficients are contained inside this circular region. Equivalently, ALL possible passive load impedances are representable by points contained inside this circular region.

Next, consider the two representations of all possible impedances with a constant real part of 50 Ω, illustrated in Fig. 3. In order to represent all loads with the same real part (50 Ω in this case), the rectangular chart contains a vertical line infinitely long. Clearly, this page isn't large enough to capture all of that line. In contrast, that constant 50 Ω line is fully captured within the Smith Chart on the right side of Fig. 3

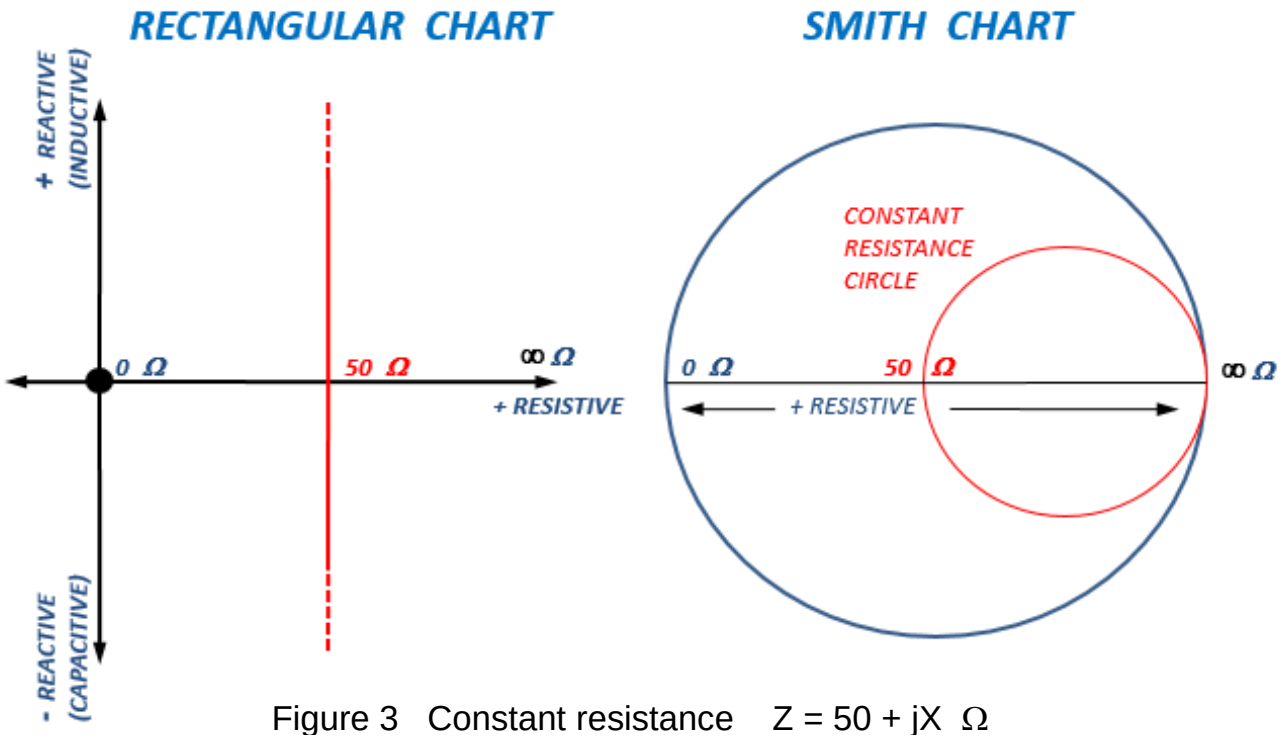


Figure 3 Constant resistance Z = 50 + jX Ω

Impedance is a complex number with a real part and an imaginary part: Z = R + jX. Impedance represents a series connection of a resistor and a reactance. A positive reactance is inductive and a negative reactance is capacitive. Constant real lines (resistances) become circles on the Smith Chart. Note also that the positive real axis from the rectangular chart maps into the horizontal line that divides the Smith Chart into upper and lower halves.

If we consider constant reactance lines, either +j 50 Ω inductive or -j 50 Ω capacitive, the rectangular chart contains an infinitely long horizontal line. This is shown in Fig. 4. The upper half of the Smith Chart represents all possible positive real, inductive impedances. Similarly, the lower half of the Smith Chart represents all possible positive real, capacitive impedances.

When more constant R and constant X lines are plotted in Smith Chart form, the impedance chart results. This is illustrated in Fig. 5.

It should again be restated that the impedance chart represents series connections. For example, if we start with a load impedance point on the chart 50 + j 50 Ω, and add a series reactance, we will obtain a new location on the same real line. Only the reactance is changed. Tuning with series LC elements stays on the same real circle.

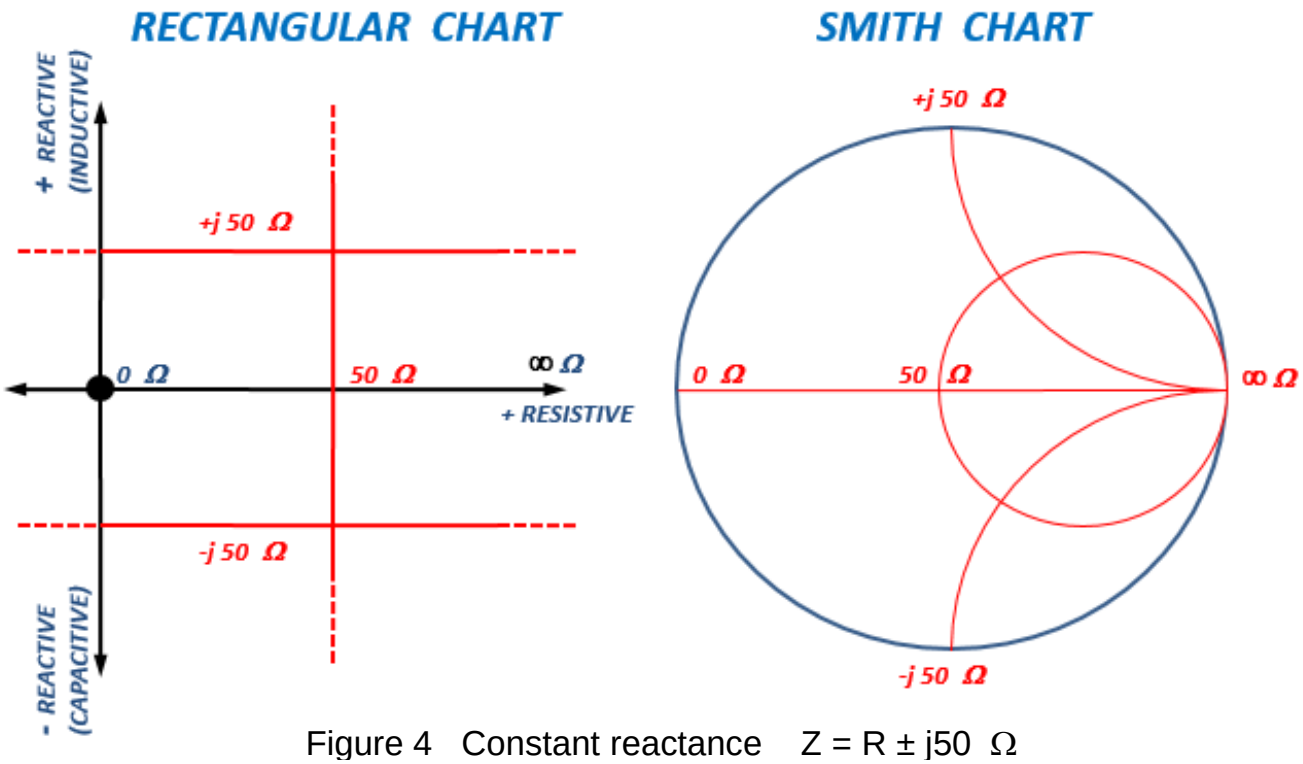


Figure 4 Constant reactance Z = R ± j50 Ω

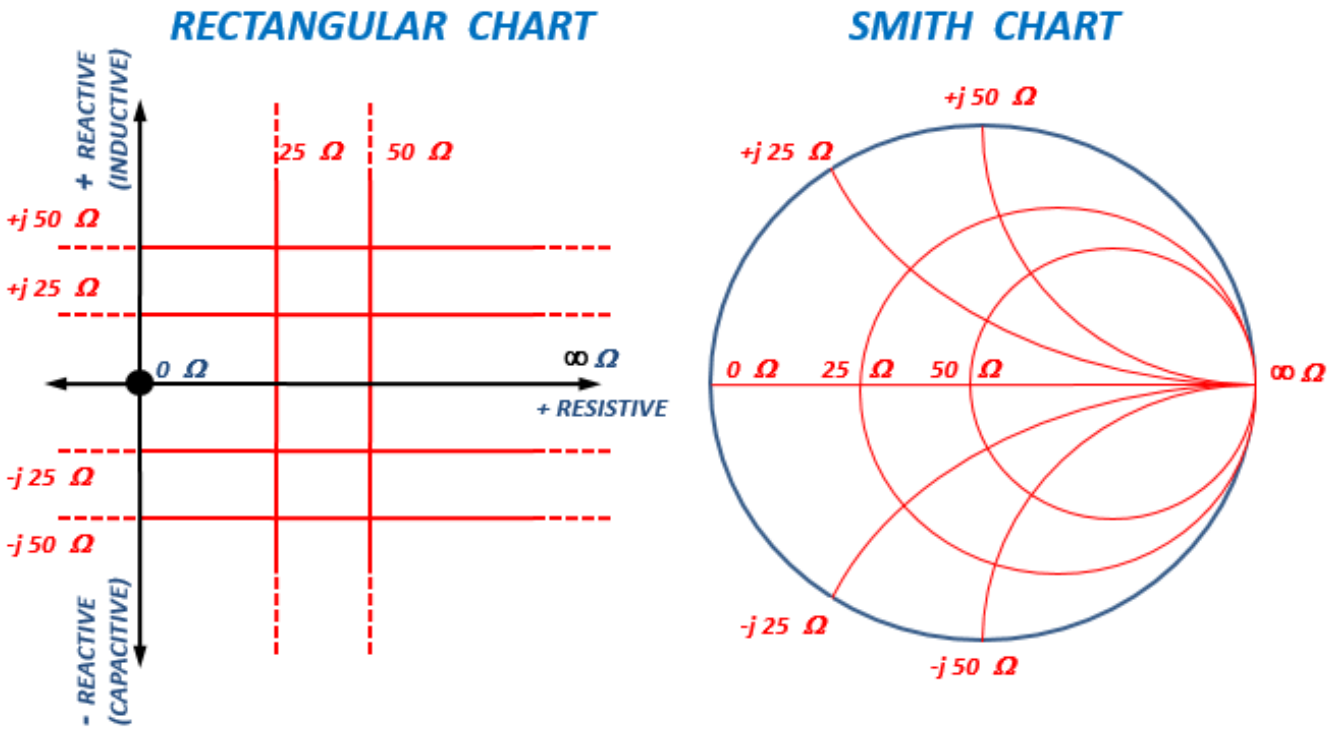


Figure 5 More constant R and X lines produce the impedance view chart

Parallel connections of resistors and capacitors or resistors and inductors are best represented in terms of admittance. Adding or subtracting parallel elements directly adds or subtracts to the admittance. Like impedance, admittance is complex with a real part called conductance (G) and an imaginary part called susceptance (B). Admittance is expressed as: Y = G +jB . Units of admittance are 1/Ω or S (Siemens). The admittance chart is shown in Fig. 6. Just as constant resistance contours are circles in the impedance chart, the admittance chart has constant conductance contours as circles. Note that the 20 mS (20 miliSiemens) circle passes through the center of the chart. The center of the chart is 50 Ω = 1/(20 mS), or alternatively 20 mS = 1/(50 Ω). Constant susceptance (imaginary part of admittance) contours are arcs similar to the constant reactance arcs in the impedance chart. The upper half of the chart is inductive (negative sign susceptance) and the lower half is capacitive. This is consistent with the nature of those regions in the impedance chart.

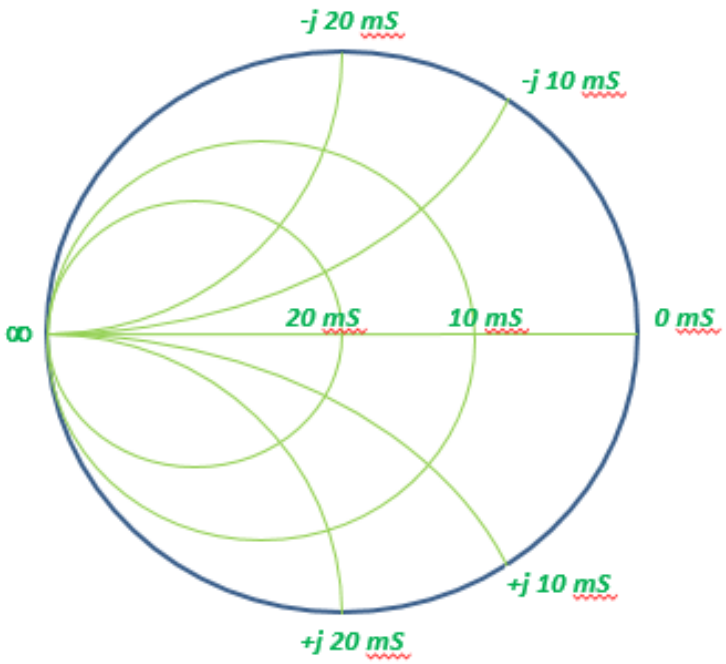


Figure 6 The admittance chart

If the impedance and admittance charts are overlaid, a very powerful tool results. This composite chart is sometimes called the immittance chart. Each point on this chart can be interpreted as a series resistance and reactance or as it's equivalent parallel form. As shown in Fig. 2, each point on the chart can also be interpreted as a reflection coefficient in a (center of chart reference) 50 Ω system. Sometimes you will see the chart published in a "normalized" form where the center of the chart is 1 instead of 50 Ω or 20mS. In that case, you will need to multiply all normalized impedance numbers by 50 and all normalized admittance numbers by 0.020.

The power of the overlaid chart is that it allows to one simultaneously switch back and forth between series and

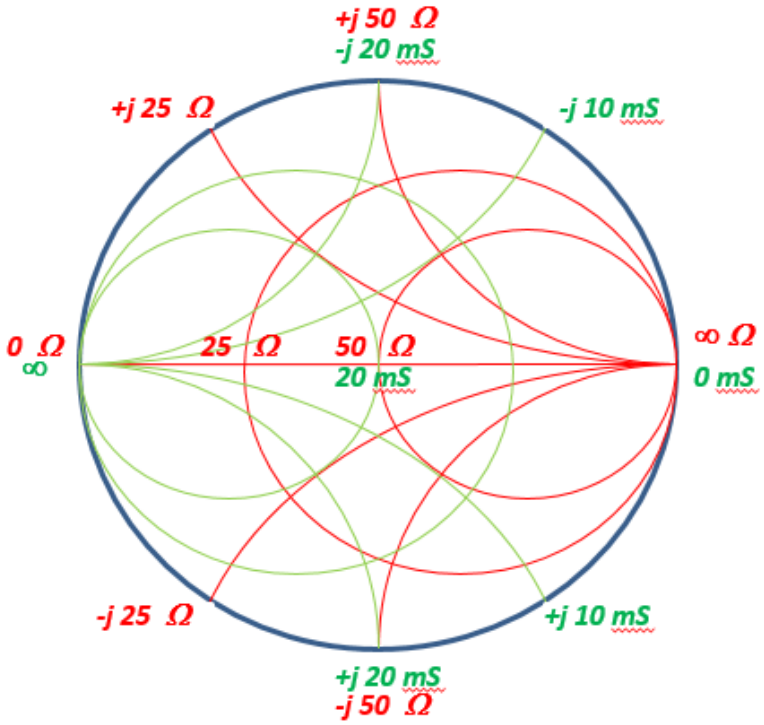


Figure 7 The immittance chart

parallel views. This will allow a matching circuit to be built element by element.

As an example of lumped element matching with the immittance chart, start with a 25 Ω load and match it to 50 Ω. In Fig. 8, the 25 Ω point, A, is on the horizontal real axis and on the constant resistance (25 Ω) circle. As inductive reactance is added, we move upward on the 25 Ω circle. If the correct amount of inductance is added, we will move to point B. Alternatively, capacitive reactance could be added to mode from A to C. Note that both A and C are on the 20 mS constant conductance circle. Next we use the parallel representation contours. By adding parallel capacitance, we can move from B, down the 20 mS circle to the center of the chart. We have a match from 25 Ω to 50 Ω with a series inductor followed by a shunt capacitor ! Similarly, a series capacitor followed by a shunt inductor path, moving from A to C to the center, could be used for an alternate matching circuit. Quantitatively, the amount of series reactance and shunt susceptance can be read directly from the chart. The L and C values are the calculated from the reactance and susceptance values. Series L or C element values are calculated from the reactance shifts as read from the Smith Chart:

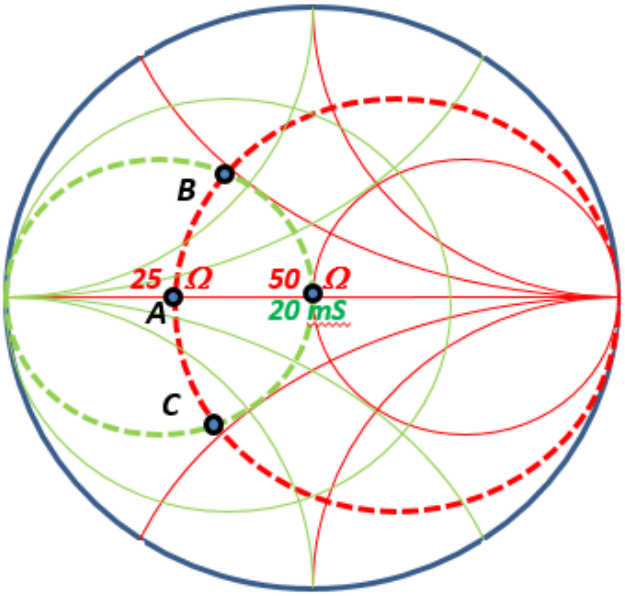


Figure 8 Lumped element matching

$L_S = \frac{|X_L|}{2\pi F}$ and $C_S = \frac{1000}{2\pi F|X_C|}$, where units are L(nH), C(pF), X(Ω) and F(GHz).

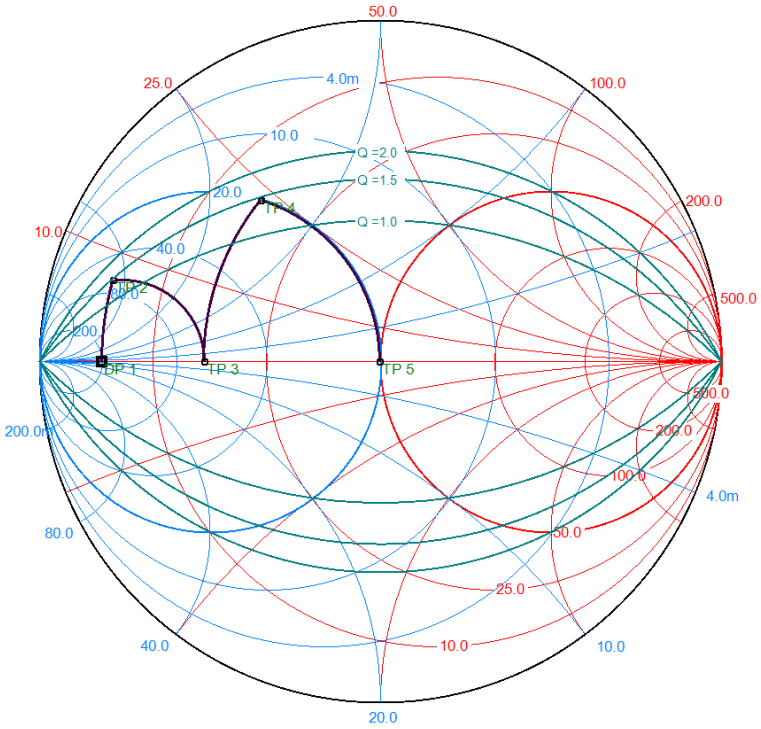
Similarly, the shunt L or C elements are calculated from the susceptance shifts as read from the Smith Chart:

$C_P = \frac{|B_C|}{2\pi F}$ and $L_P = \frac{1000}{2\pi F|B_L|}$, where units are L(nH), C(pF), B(mS) and F(GHz).

Examples of larger transformation matches can be seen in Figs. 9 and 10. In both of these examples, two section (4 element) matches are used to match 5 Ω to 50 Ω. Figure 9 does this with two lowpass sections (series L, shunt C, series L, shunt C). Figure 10 does this with a lowpass and a highpass section (series L, shunt C, series C, shunt L) to achieve a bandpass response. In both cases, the first section matches 5 Ω to 15.8 Ω and the second section matches 15.8 Ω to 50 Ω.

In addition to the immittance chart, please note the constant Q (= 1.5) “football” shaped contours. It is important to maintain the low and similar loaded Q in both match sections. This will allow a similar loss to be achieved in each. The lower the loaded Q of a matching section, the lower the loss. Losses in lumped matching circuits are due primarily to series resistance in inductors. Losses in capacitors are typically much lower than in inductors. A useful measure of inductor loss is Qu, the unloaded Q. The insertion loss of a two element section is expressed

mathematically as: $\text{Loss(dB)} = 20\ \log_{10}\left[\frac{(Q_U - Q_L)}{Q_U}\right]$. Clearly, high Q_U inductors provide low circuit losses.



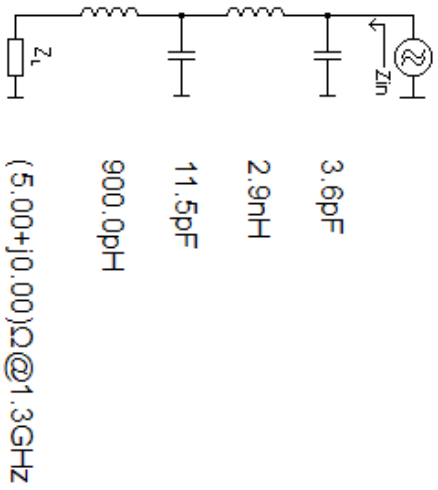
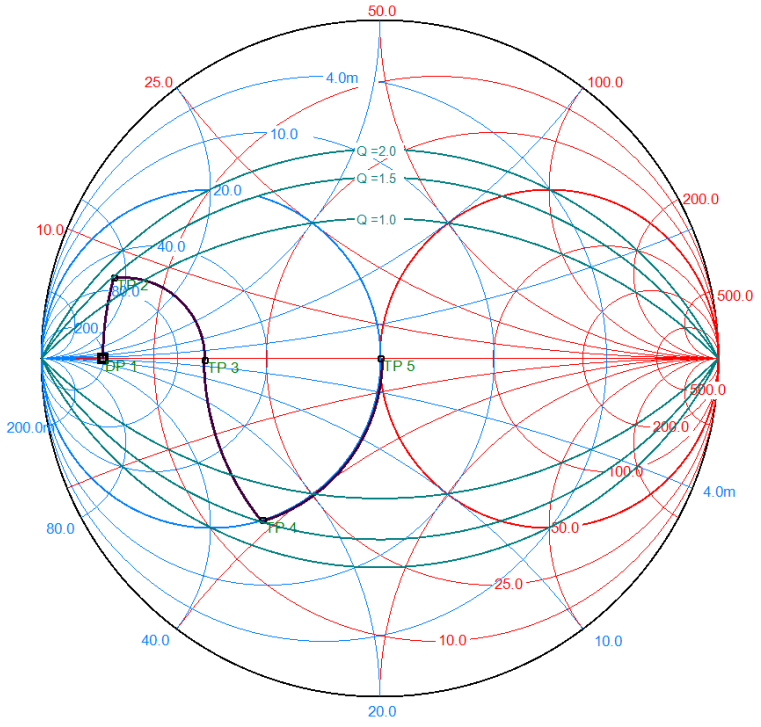


Figure 9 LsCpLsCp LP match



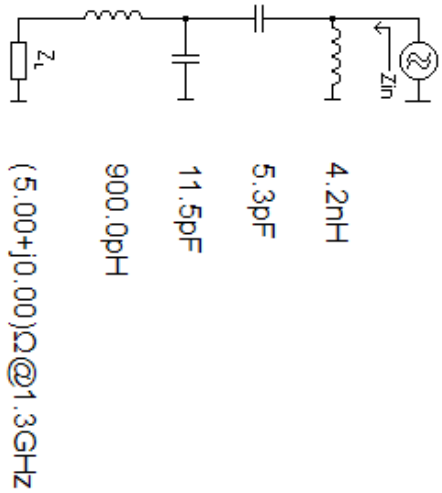


Figure 10 LsCpCsLp BP match

Figures 9 & 10 were generated using the software tool ***Smith***:
http://www.fritz.dellsperger.net/smith.html.

In general, it is useful to view larger LC ladder structures as cascades of two element LC sections. The loaded Q of each section determines the real transformation (as in a transformer) of that section, by a factor of $[1 + Q_L^2]$. If we wish to limit the loaded Q in the circuit for more bandwidth and lower insertion loss, then more than one section may be required to achieve the overall transformation needed. This is seen in both Figs. 9 and 10 where the two sections allowed the loaded Q to be limited to 1.5. Alternatively, a single section match from 5 Ω to 50 Ω would require a loaded Q of 3. ($10 = 1 + 3^2$).

Naturally, the question arises as to how many matching elements will yield the lowest loss. That trade-off can be seen in Fig. 11 for a range of transformation ratios and inductor Q. For example, plotted in blue are 2, 4 and 6 element cases with an inductor unloaded Q of 10. The 2 element (single section) curve crosses the 4 element (2 section) case at a transformation ratio of 6. This tells us that it is preferable to use two sections (4 elements) when inductor Q is 10 and the desired transformation is greater than 6x.

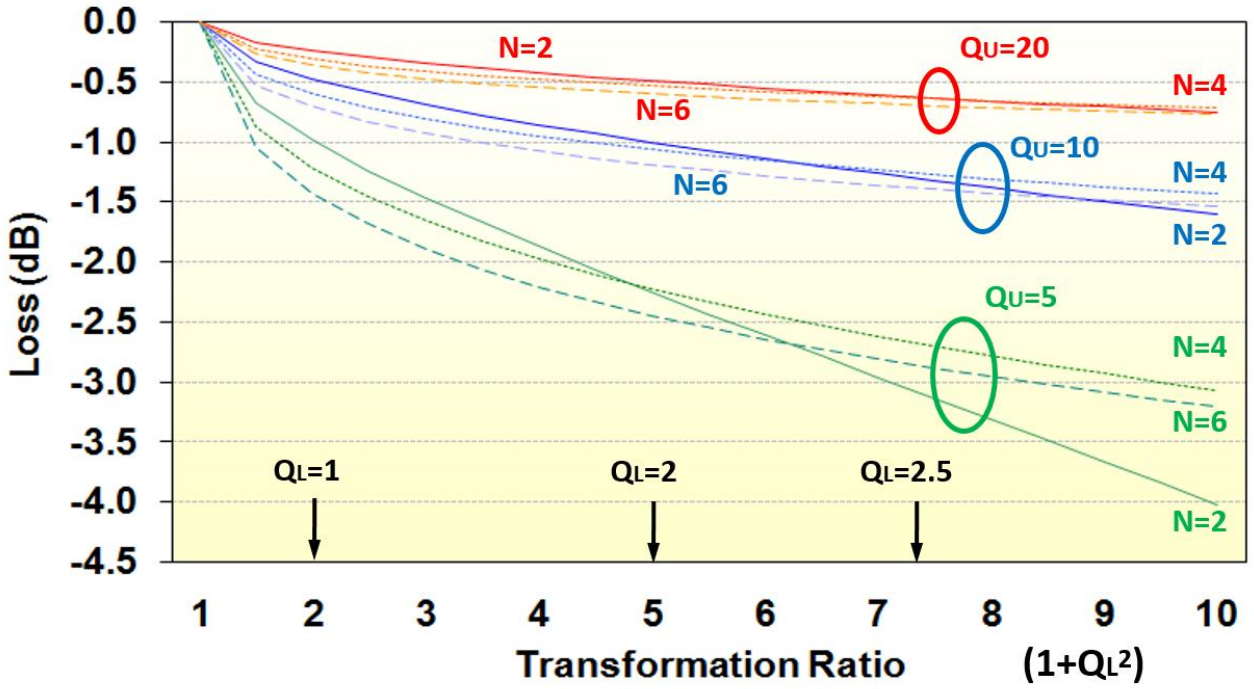


Figure 11 Insertion loss vs transformation ratio and inductor Q

REALIZATION OF A LUMPED DESIGN ON A CIRCUIT BOARD

Let's begin with a bold statement: "There are no truly lumped circuit elements." Chip capacitors have series inductance associated with the package length. Even a small parasitic inductance will eventually resonate the capacitor if the frequency is raised high enough. Similarly, chip inductors have parasitic shunt capacitance that cause a natural self-resonance at some (high) frequency. Chip resistors have series inductance and shunt capacitance due to the non-zero dimensions. Copper traces on a PC board over a back side ground-plane form a quasi-TEM transmission-line called microstrip. That said, its behavior could be approximated by a cascade

of small series inductors and shunt capacitors. The ratio of incremental inductance to incremental capacitance sets the characteristic impedance as: $Z_0 = \sqrt{\frac{L}{C}}$.

The approach here will be to use short (< 30° or < λ/12) segments of microstrip line to represent series inductors. This is done by using high characteristic impedance where the ratio of incremental series inductance to shunt capacitance is high. Physically, these lines are narrow compared to board thickness.

Short segments of wide traces where the Z_0 is low, represent predominantly shunt capacitance. Pads for chip capacitors fall into this category; so, a circuit node where a shunt capacitor is desired must take into account both the pad capacitance and the effective capacitance of the chip cap. Since, in simplest terms the chip cap is represented as a capacitor in series with a small inductance (due to the body length), the effective capacitance is based on the net X_C of the chip at the operating frequency.

The approach used here is to approximate PC board traces as 3 element LC equivalent circuits. Low Z_0 (wide) lines are represented as a T circuit and high Z_0 (narrow) lines are represented as π circuits. This is a very powerful technique both for estimating chip component parasitics and for realizing printed inductors. This 3rd order lumped LC representation of a length of transmission line is shown in Fig. 12.

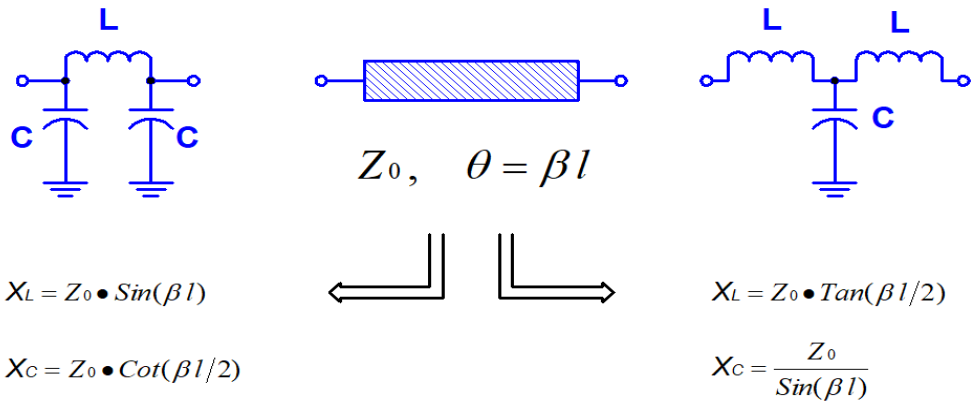


Figure 12 LC representation of a short transmission line

The author has written a software tool that combines the microstrip calculations and the 3rd order equivalent circuit calculations. A windows executable can be downloaded at: http://k5tra.net/TechFiles/LumpEquiv.exe . This will make performing the necessary calculations painless. Depending on your windows OS version, you may also need to install vbrun32.dll, a runtime library (usually not necessary on newer PCs). Another useful calculator allows calculation of the effective capacitance of series LC branches (like a chip cap). That tool gives effective capacitance at fundamental, second, and third harmonic frequencies. If a resonance is passed, it will give the effective inductance. This windows executable can be downloaded at: http://k5tra.net/TechFiles/SeriesTrap.exe . Figure 13 shows a screen display from both of these tools.

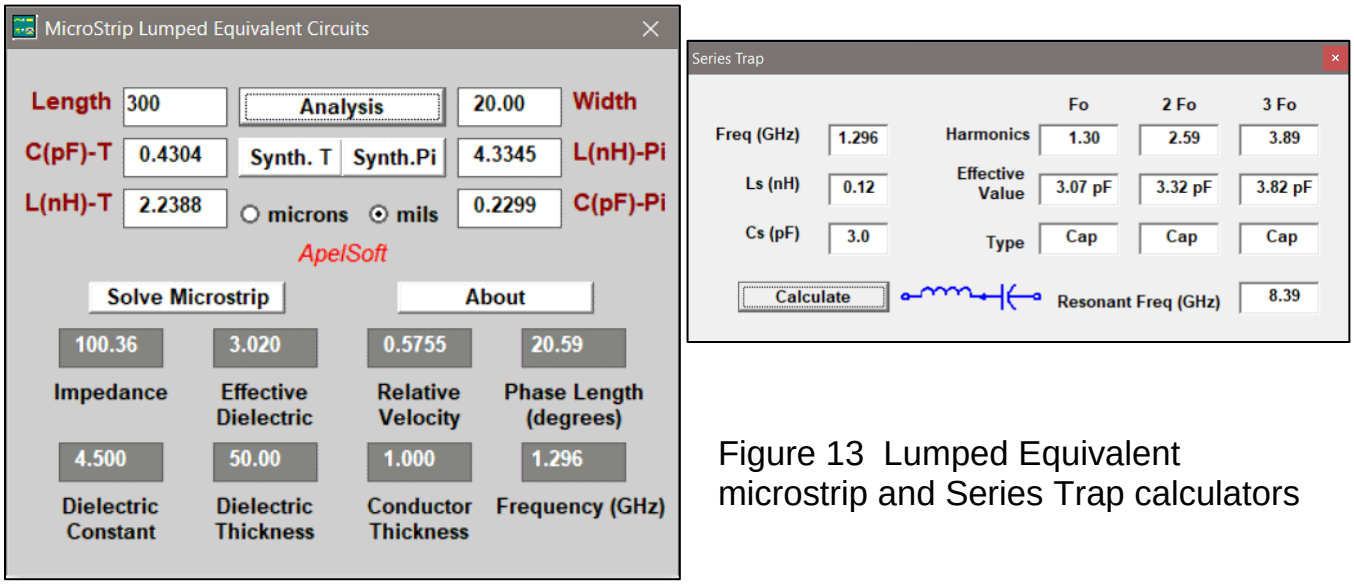


Figure 13 Lumped Equivalent microstrip and Series Trap calculators

Before we work through a design example, it is worth pointing out that a useful estimate of the self-inductance of various surface-mount chips can be made with the microstrip lumped equivalent calculator by loading the package footprint length and width. These results, over a 50 mil FR-4 substrate are shown in Fig. 14. This suggests that an 0603 3pF capacitor is used at 1296 MHz, it will actually look like a 3pF cap in series with 0.77 nH. The Series Trap calculator indicates that the effective capacitance at 1296 MHz is 3.54 pF and at the second harmonic (2596 MHz) it is 7.75 pF. It also indicates series resonance at 3.31 GHz.

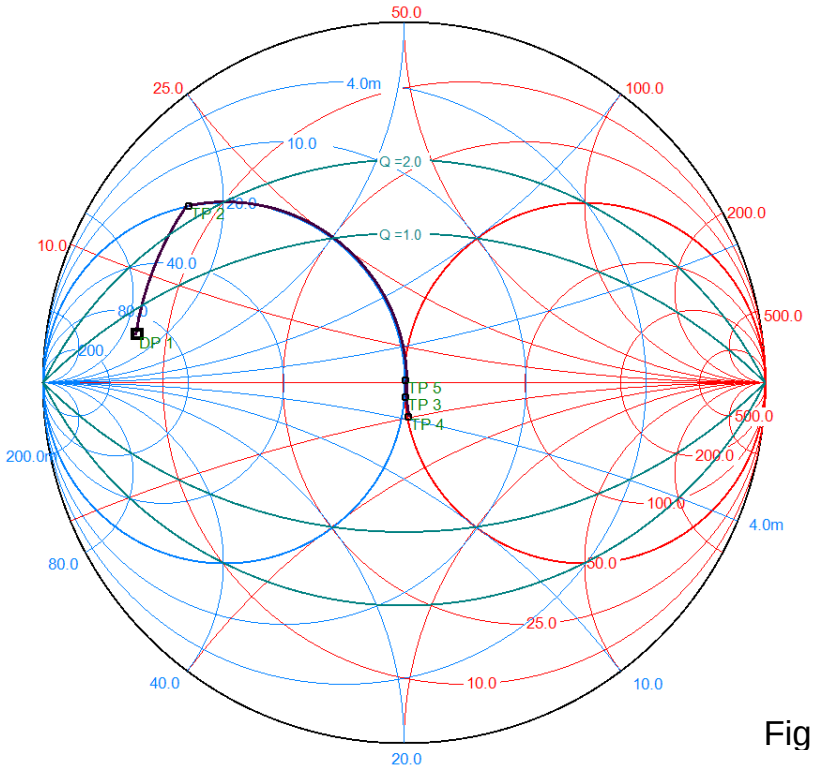
CHIP PKG	DIM (mil^2)	L(nH)
0402	40x20	0.59
0603	60x30	0.77
0805	80x50	0.84
ATC 100A	55x55	0.55
ATC 100B	110x110	0.77

Figure 14 SMD series inductance

A DESIGN EXAMPLE

To illustrate the design procedure, let's use a SGA-9189 SiGe transistor to make a 1296 MHz driver stage. This will produce 25 dBm, sufficient to drive a power module. The optimum source and load impedances to present to the transistor base and collector are: $Z_S = 7.1 - j\,4.4\ \Omega$ and $Z_L = 18.4 + j\,4.1\ \Omega$. If the matching networks are to provide these optimum impedances, then the complex conjugate impedances can be used as a starting point load in the design of the matching circuits. A reflection match will be a conjugate match. So, the input matching circuit should be designed to interface to a load of: $Z_S^* = 7.1 + j\,4.4\ \Omega$, and the output matching circuit should be designed to interface to a load of: $Z_L^* = 18.4 - j\,4.1\ \Omega$.

As a first step, simple lumped LC matching circuits are designed with the complex conjugated optimum impedances as terminations. These can be seen in Figs. 15 and 16.



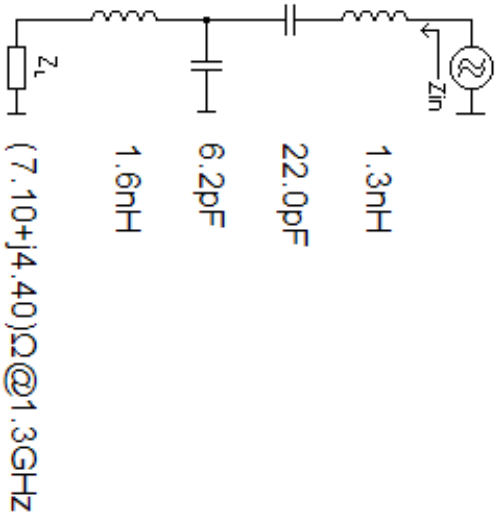
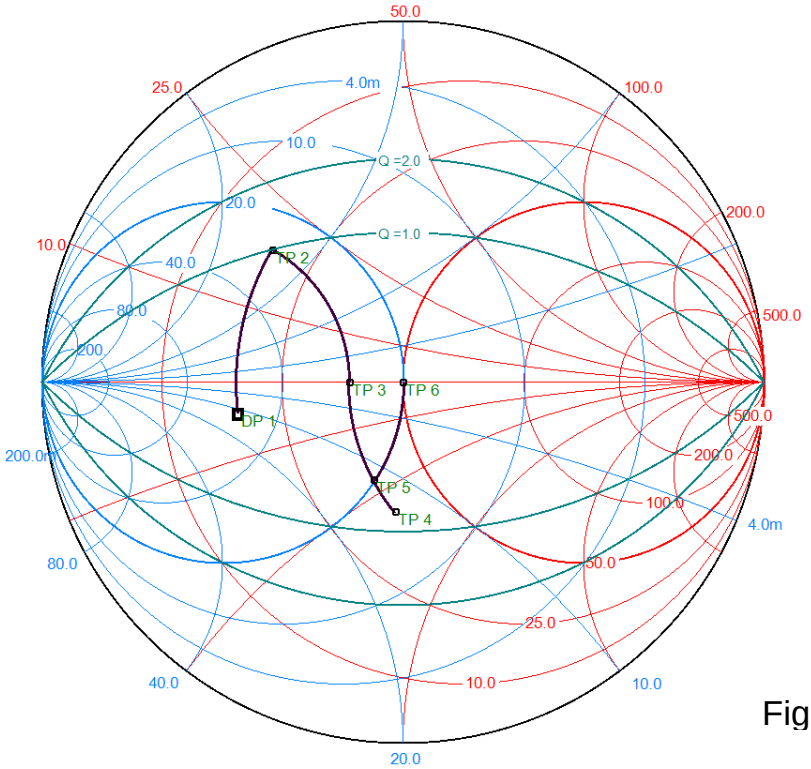


Figure 15 SGA-9189 LC input match



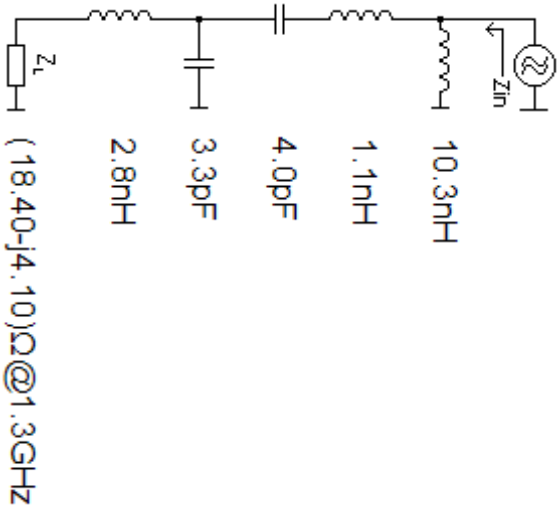


Figure 16 SGA-9189 LC output match

INPUT MATCH ON FR4 BOARD

The input match is a single section Ls, Cp, followed by a 22 pF series DC block capacitor. An additional series inductance around 1 nH was included in anticipation of the parasitic series inductance of the series chip capacitor. The initial series inductance of 1.6 nH can be represented by a 40 mil wide trace on a 50 mil thick FR4 circuit board. This width forms a 77 Ω microstrip line. From the Lumped Equivalent calculator, find that a length of 139 mils is equivalent to a 1.6 nH inductor with 0.136 pF parasitic shunt capacitance at each end. This is shown in Fig. 17.

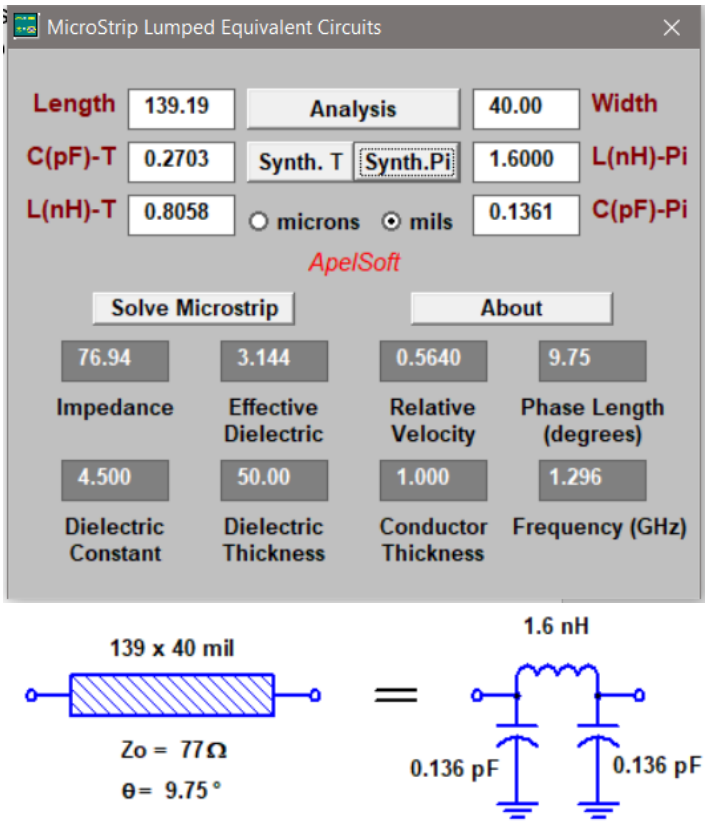


Figure 17 1.6 nH from 77Ω microstrip

Following the 1.6 nH inductor is a 6.2 pF capacitor (Fig.15). The 0.136 pF parasitic capacitance from the 77 Ω line will account for a very small part of this. Additionally, a shunt chip cap will need to supply the remaining 6.064 pF with it's effective capacitance (series LC equivalent). A 0805 chip will have approximately 0.84 nH of self inductance. A 0.035 diameter plate through hole will contribute another 0.52 nH. After a couple calculations with the Series Trap calculator, we find that a 3.9 pF cap in series with 1.4 nH has an effective capacitance of 6.1 pF at 1296 MHz. This is a good solution with a standard value cap and the series inductance that must be absorbed.

To summarize, the input match is comprised of a 139 mil long x 40 mil wide trace, a shunt 0805 3.9 pF chip cap to ground, and a series 0805 22 pF capacitor to the RF input signal (50 Ω port). This partial layout can be seen in Fig. 18. Note that the shunt 3.9 pF cap is located in the correct design position, with some position tunability provided in the layout. The region on the transmission line and on the adjacent ground metal where the capacitor could be placed should be defined as exposed 'pad' metal (cleared of solder mask).

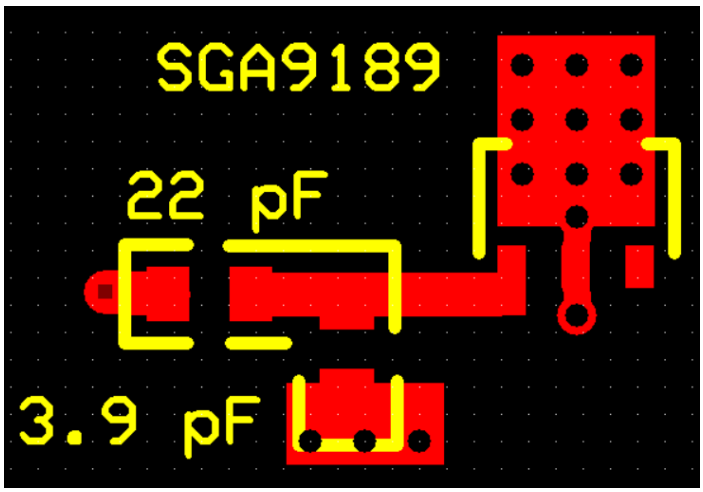
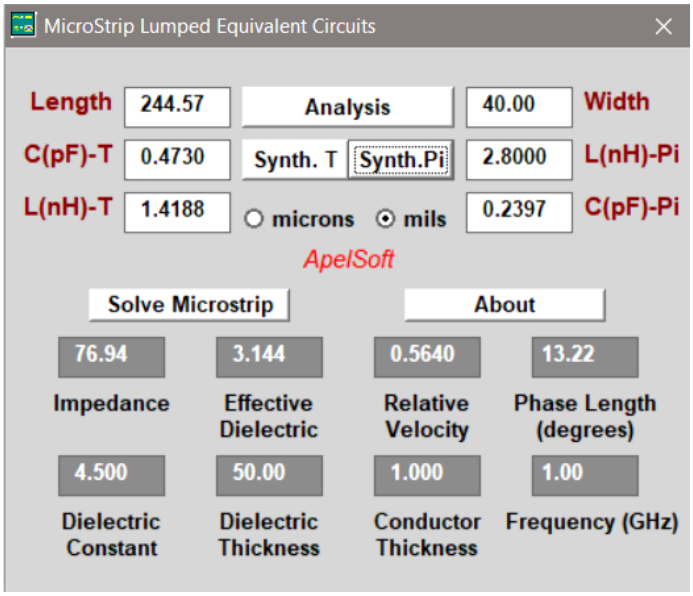


Figure 18 Input RF impedance match

OUTPUT MATCH ON FR4 BOARD

The output match is a two section Ls, Cp, Cs, Lp match. The Cs branch provides DC blocking of collector bias voltage. As in the input match, a series inductor around 1 nH is places in series with the series 4.0 pF capacitor, in anticipation of the self-inductance of a chip capacitor.

The initial series inductance of 2.8 nH, will again be represented by a 40 mil wide trace, 77 Ω microstrip line. From the Lumped Equivalent calculator, find that a length of 245 mils is equivalent to a 2.8 nH inductor with 0.24 pF parasitic shunt capacitance at each end. This is representation is shown in Fig. 19.



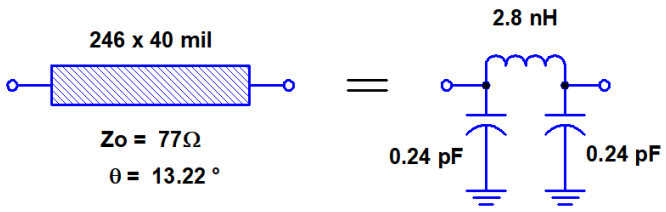
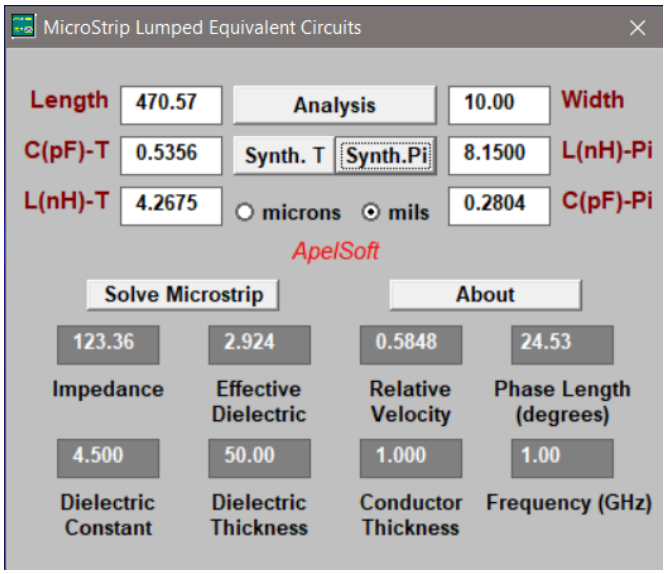


Figure 19 2.8 nH from 77Ω microstrip

The 3.3 pF shunt capacitor is contributed to by the 0.24 pF parasitic shunt C at the end of the 77 Ω line. So the desired capacitance becomes 3.06 pF. As in the input match, the self-inductance of the shunt chip cap and the ground via hole accounts for approximately 1.4 nH. Once again, the Series Trap calculator yields a 3.09 pF effective capacitance from a series 2.4 pF and 1.4 nH at 1296 MHz.

The next element in the output match is 4 pF capacitance in series with 1.1 nH. After the 0.84 nH self-inductance of an 0805 chip cap is absorbed, a residual 0.26 nH remains to be realized in the layout.

All that remains to be realized is the 10.3 nH shunt inductor. This is considerably more than the previously used inductors. An increase in characteristic impedance (>77Ω) of the microstrip line will provide more inductance per unit length. A 10 mil wide line forms a 123 Ω line. The Lumped Equivalent calculator yields a solution of 634 mils long for an equivalent circuit of 10.3 nH with parasitic shunt capacitances of 0.39 pF at each end. That much shunt capacitance across the inductance will produce an effective inductance that is around 14 nH; so we will need to reduce the length of this line. This effective inductance of an LC parallel connection is analogous to the effective capacitance we encountered earlier in series LC branches representing a capacitor. That said, you will probably also want to download the ShuntTrap calculator at: http://k5tra.net/TechFiles/ShuntTrap.exe . This tool will allow you to easily find that 8.67 nH in parallel with 0.28 pF is equivalent to 10.3 nH at 1296 MHz. The Lumped Equivalent calculator provides the physical solution for this as: 470 mils x 10 mils (8.15 nH). The total 8.67 nH = 8.15 nH + 0.52nH via inductance. This solution is shown in Fig. 20.



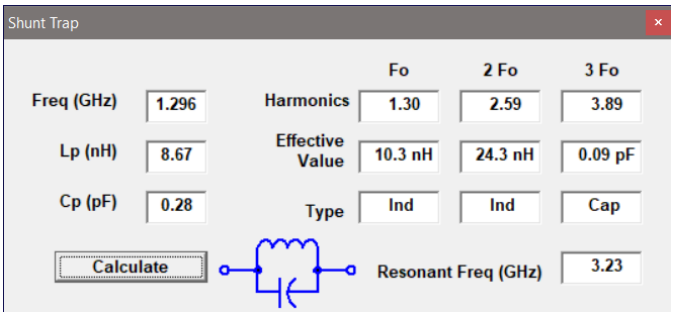


Figure 20 10.2 nH solution with Lumped Equivalent and Shunt Trap calculators

In summary, the output match is comprised of a 246 mil long x 40 mil wide trace, a shunt 0805 2.4 pF chip cap to ground, followed by a series 0805 4 pF capacitor and a shunt 470 mil x 10 mil transmission line to ground through a 35 mil via (total approximates 10.3 nH). The RF output input signal (50 Ω port) is at the junction of the 4 pF series cap and the shunt 478 mil line. This partial layout can be seen in Fig. 21. Note that the shunt 2.4 pF cap is located in the correct design position, with some position tunability provided in the layout. The region on the transmission line and on the adjacent ground metal where the capacitor could be placed should be defined as exposed 'pad' metal (cleared of solder mask).

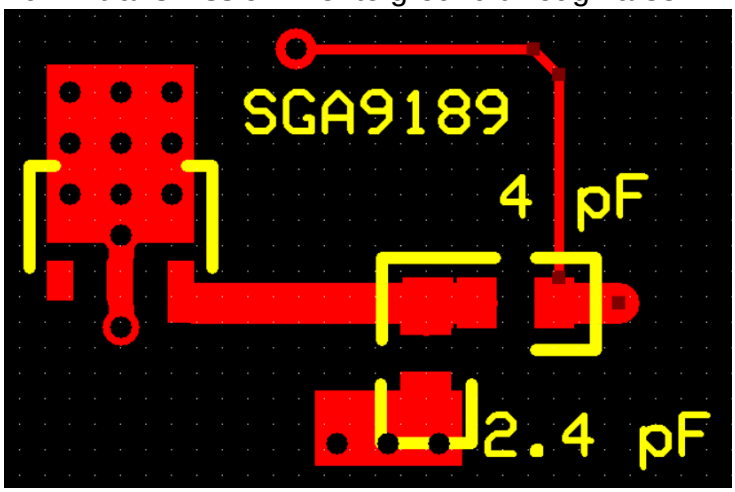


Figure 21 Output RF impedance match

CONCLUSIONS

A methodology for realizing board level impedance matching circuits has been presented including a design example at 1296 MHz. This methodology includes utilizing board microstrip traces to approximate inductors from a lumped LC design. Additionally, a methodology to design lumped LC matching circuits with the Smith Chart was presented. An overview of the Smith Chart was also presented as an initial part of that discussion. Load Q and the Q·BW product was briefly discussed, due to the importance of Q_L in setting the limits of achievable impedance match performance. A number of software tools were highlighted in this paper. The K5TRA software tools are free and downloadable from http://k5tra.net . The Smith tool is not

free; but it is well worth the small expense. Smith is available from: http://www.fritz.dellsperger.net/smith.html.

The overall layout of the SGA9189 amplifier is illustrated in Fig.22, including bias feed lines. Some degree of tunability was built-in to the layout. Line junction and step discontinuities were not included in this paper, as they were minimal in the example design and outside the intended scope of the paper.

It is hoped that the approach presented here will stimulate more board level RF home brewing.

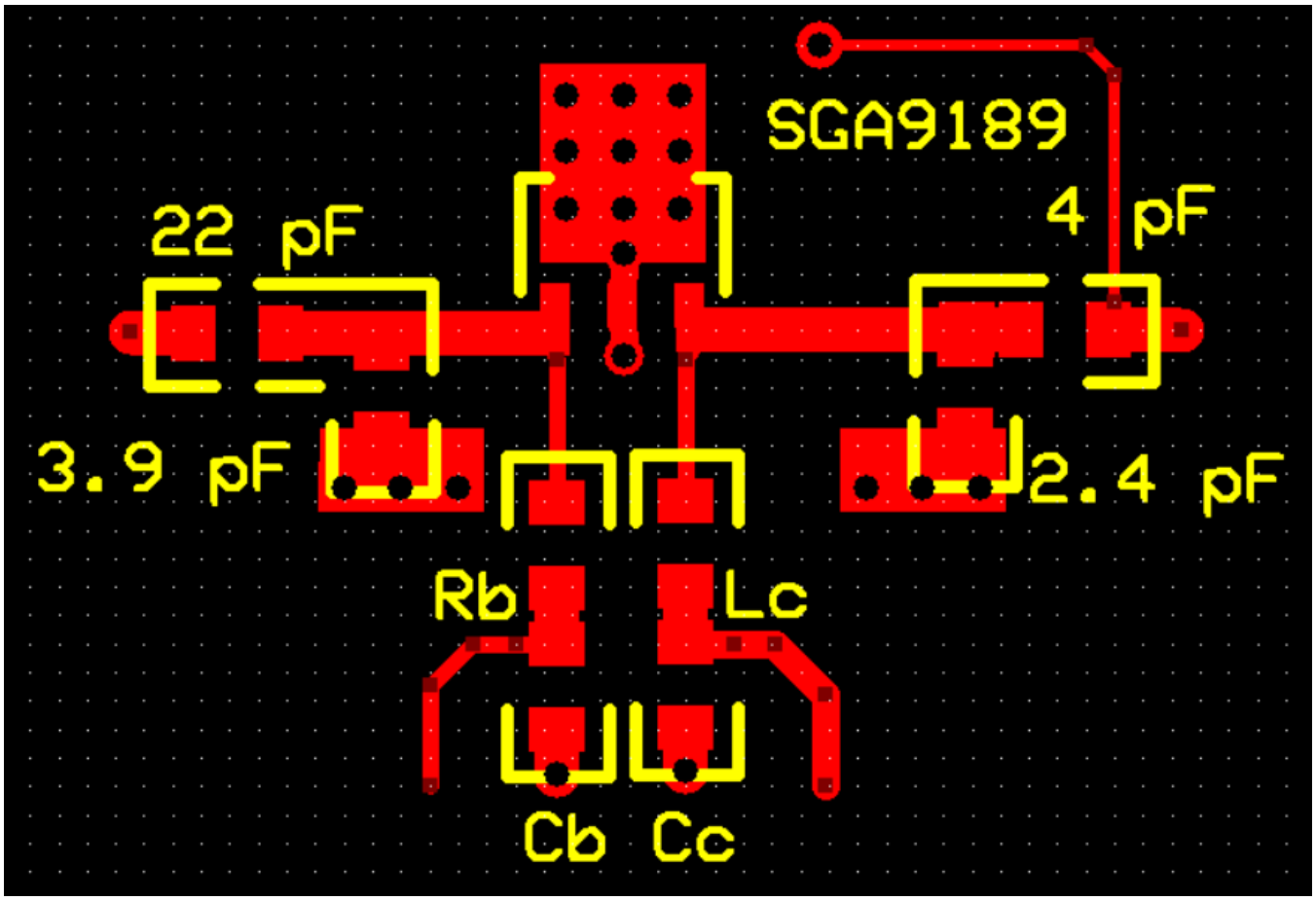


Figure 22 Overall SGA-9189 amplifier layout